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(54) Title: MASSIVELY PARALLEL INTERFACE FOR ELECTRONIC CIRCUIT

(57) Abstract: Several embodiments of massively parallel interface structures are disclosed, which may be used in a wide variety of permanent or temporary applications, such as for interconnecting integrated circuits (ICs) to test and burn-in equipment, for interconnecting modules within electronic devices, for interconnecting computers and other peripheral devices within a network, or for interconnecting other electronic circuitry. Preferred embodiments of the massively parallel interface structures provide massively parallel integrated circuit test assemblies. The massively parallel interface structures preferably use one or more substrates to establish connections between one or more integrated circuits on a semiconductor wafer, and one or more test modules. One or more layers on the intermediate substrates preferably include MEMS and/or thin-film fabricated spring probes. The parallel interface assemblies provide tight signal pad pitch and compliance, and preferably enable the parallel testing or burn-in of multiple ICs, using commercial wafer probing equipment. In some preferred embodiments, the parallel interface assembly structures include separable standard electrical connector components, which reduces assembly manufacturing cost and manufacturing time. These structures and assemblies enable high speed testing in wafer form.